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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,321	03/06/2002	Makoto Kanbe	1035-371	7734

7590 08/05/2004

Nixon & Vanderhye P.C.
8th Floor
1100 N. Glebe Rd.
Arlington, VA 22201

EXAMINER	
NGUYEN, JIMMY H	

ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 08/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,321	KANBE ET AL.	
	Examiner	Art Unit	
	Jimmy H. Nguyen	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2004 and 18 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18,20,23,31,33,41 and 45-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *49* is/are allowed.

6)☒ Claim(s) *18,20,23,31,33,41 and 46-48* is/are rejected.

7)☒ Claim(s) *45* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 08/974,496.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 06/01/2004 has been entered. Claims 18, 20, 23, 31, 33, 41 and 45-49 are currently pending in the application. An action on the RCE follows:

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 18, 20, 23, 31, 33, 41 and 46-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasui et al. (USPN: 5,248,963), hereinafter Yasui, and further in view of Tsuboyama et al. (USPN: 5,592,191), hereinafter Tsuboyama.

Regarding to claims 18 20 and 23, the claimed invention reads on Yasui as follows: Yasui discloses an erasing device for a LCD device (fig. 3) having a LCD panel (10) whose pixels are driven by active elements (13), for erasing a display image on said LCD panel when a power source of a main body of said LCD device is turned off, the erasing device comprising a **power source OFF detecting circuit** (a voltage drop detector 24, fig. 5, abstract) for detecting the turning off of the power source of the main body of LCD device, **a power source control**

circuit (a circuit including elements 22, 23, 25, 26, 27 and an inherent circuit for providing signals D, PCK and M, see figs. 3 and 5) including a power holding circuit 22 for maintaining power to the LCD panel for a certain period after the power source is turned off (col. 4, lines 50-53), and **an erasing circuit** (a circuit including elements 16, 17 and an inherent opposing electrode circuit for providing a signal to a common electrode 12b, figs. 3 and 5) for applying an OFF-level voltage (a voltage level corresponding to pixel data D of logic "0", col. 3, lines 58-60), using the power supplied by the power holding circuit 22 of the power source control circuit, to all pixels in the LCD panel, thereby erasing the display in a short time after the turning OFF of the power supply (figs. 3 and 5, col. 3, lines 1-22 and lines 58-67). Yasui further discloses the erasing circuit including **a source driver** (a source bus driver 16b, best seen fig. 1), **a source driver control circuit** (a circuit including a plurality of shift registers 16a, fig. 1), for providing signals to control the source driver (16b), and an inherent opposing electrode control circuit for outputting an opposing electrode signal (a voltage) to opposing electrodes (common electrodes 12b) (fig. 3, col. 3, lines 58-67). Yasui further teaches the power source control circuit providing signals D, PCK and M to the source driver control circuit (16a), thereby controlling the source driver control circuit (16a), and controlling the opposing electrode control circuit. Yasui further teaches the erasing circuit applying to both the pixel electrode (12a) and the opposing electrode (12b) an OFF-level voltage (the common potential EG of zero volt, col. 1, lines 58-59) within time T and a negative voltage E2 latter (col. 1, lines 58-60 and col. 6, lines 3-9). Accordingly, the Yasui reference discloses all the claimed limitations except that the Yasui power source control circuit does not output to the source driver control circuit (16a) a source enable signal which is at a selecting level during the certain period T.

However, Tsuboyama discloses a related erasing device for a LCD, the power source control circuit (a circuit including elements 104 and 105, see fig. 1) including a logic control unit (107), for outputting a source enable signal (a data side Vc control signal, fig. 1), which is at a selecting level (a low level) during the certain period TE (fig. 5A), to the source driver control circuit (shift register/latch circuit 25, fig. 2) which, in response to the source enable signal, to cause the source driver (a circuit including switching array 22, fig. 2) to provide a voltage V4 to the pixel electrode, thereby turning off the LCD (fig. 5A, col. 4, lines 37-60). It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to provide the logic control unit 107 in the Yasui power source control circuit, in view of the teaching in the Tsuboyama reference, because this would eliminate image disturbance from a display panel even when power is turned off, and enable uniform orientation of the liquid crystal, as taught by Tsuboyama (col. 1, line 64 through col. 2, line 27).

Regarding to claims 31 and 33, Yasui fails to teach the active matrix type LCD device including a reflective LCD device or a Guest-Host LCD device. Official Notice is taken that the active matrix type LCD device including a reflective LCD device or a Guest-Host LCD device is notoriously well known and expected in the art. Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to have the active matrix type LCD device of Yasui including a reflective LCD device and a Guest-Host LCD device as these displays are known to consume less power since these displays operates without using a backlight.

Regarding to claims 41, 46 and 47, as discussed above, Yasui teaches the erasing means outputting a voltage signal (E2) to both pixel electrode (12a) and opposing electrode (12b), by

means of the source driver (16b) and the opposing electrode signal control circuit (fig. 3, col. 3, line 58 through col. 4, line 16). Yasui further discloses the erasing means including a gate driver (a gate bus driver 19) for outputting a gate driving signal (outputs G1, G2, ..., Gm), which turns on gate lines (15_1-15m) sequentially to turn on the active elements (TFTs 13) per line and a gate driver control circuit (a circuit including elements 18 and 20) (see fig. 4) for receiving a gate enable signal (a clear signal CL, fig. 4), as a starting signal for the gate driver, so that a gate driving signal (G1, ..., Gm) is outputted to gate lines (15_1-15m) (see figs. 2 and 4).

Regarding to claim 48, Yasui further discloses that, during the erasing period (T), the gate driving signal (G1, G2, ..., Gm) is fixed at a high level (col. 4, lines 3-11).

Allowable Subject Matter

4. Claim 45 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Claim 49 is allowed.

6. The following is a statement of reasons for the indication of allowable subject matter: the claimed invention is directed to an erasing device for a LCD panel whose pixels are driven by active elements, for erasing a display image on said LCD panel when a power source of a main body of said LCD device is turned off. Claims 45 and 49 identify the uniquely distinct feature, "said erasing circuit applies during the certain period a first rectangular periodic wave signal to said pixel electrode while applying a second rectangular periodic wave signal which is in a same phase and at a same level as those of the first rectangular periodic wave signal to said opposing electrode" recited in claims 45 and 49, last 4 lines. The closest art, as discussed in the rejection

above, Yasui further teaches the erasing circuit applying to both the pixel electrode (12a) and the opposing electrode (12b) an OFF-level voltage (the common potential EG of zero volt, col. 1, lines 58-59) within time T and a negative voltage E2 latter (col. 1, lines 58-60 and col. 6, lines 3-9), fails to anticipate or render the above underlined limitations obvious.

Response to Arguments

7. The amendment to claim 18 overcomes the drawing objection and the rejection under 35 USC 112, first paragraph, in the final Office action dated 03/04/2004, the drawing objection and the rejection under 35 USC 112, first paragraph, are hereby withdrawn.

8. Applicants' arguments, see pages 8-9 of the amendments filed 04/23/2004 and 06/18/2004, with respect to the rejection of claim 49 have been fully considered and are persuasive in view of the amendment to claim 19. The rejection to claim 49 in the final Office action dated 03/04/2004 has been withdrawn.

9. Applicants' arguments, have been considered but are moot in view of the new ground(s) of rejection. See the new ground (s) of rejection above.

10. Applicants' arguments with respect to independent claim 18, pages 10-14 of the amendment filed on 04/23/2004 have been fully considered but they are not persuasive.

i. Applicants argue that the gate driver power circuit shown in fig. 5 of Yasui is not a power source to the source driver. See page 10, lines 12-13. Examiner agrees because as discussed in the rejection above, the claimed power source control circuit corresponds to a circuit which includes elements 22, 23, 25, 26, 27 and an inherent circuit for providing signals D, PCK and M, to the source driver control circuit (16a). See figs. 3 and 5.

ii. Applicants argue that Yasui teaches away by disclosing **turning OFF** the gate driver to the pixels. See page 10, lines 15-16. Examiner disagrees because, as noting in the abstract, last 5 lines, and the description at col. 4, lines 3-16, Yasui expressly teaches that during a certain period of time T, the gate driver **turns ON** all pixels, and the source driver applies an OFF voltage to all pixels, thereby erasing the display image.

iii. Applicants argue that Tsuboyama does not relate to active element displays. See page 11, last paragraph. It is noted applicants that the main reference, Yasui, expressly teaches an active matrix LCD device, and Tsuboyama discloses an matrix LCD device, i.e., both Yasui and Tsuboyama disclose LCD device. Further, a teaching in the Tsuboyama reference, which is utilized in the Yasui reference, does not relate to the structure of the LCD panel (i.e., either an active matrix LCD panel or a simple matrix LCD panel), but simply just relates to a power source control circuit providing a source enable signal to control the source driver control circuit during an erasing period.

iv. Applicants argue that Tsuboyama discloses the data side Vc control signal in fig. 5 is HIGH only during the periods TVc1 and TVc2 and LOW during the erase period TE, while claim 18 uses a source enable signal which is at a selecting level during a certain period in which the liquid crystal is turned off. See page 12, last 6 lines. Examiner agrees; however, Tsuboyama expressly teaches a data side Vc control signal (i.e., the claimed source enable signal) which is at a LOW level (i.e., the claimed selecting level) during an erasing period (i.e., the claimed certain period) in which the liquid crystal is turned off. Furthermore, the claimed feature, "a selecting level", does not limit that the level must be

HIGH. Although the claim is interpreted in light of the specification, limitation from the specification is not read into the claim.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy H. Nguyen whose telephone number is (703) 306-5422. The examiner can normally be reached on Monday - Thursday, 8:00 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached at (703) 305-4938.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

JHN
July 27, 2004

Jimmy H. Nguyen
Examiner
Art Unit: 2673